IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1. (Currently Amended) A method of displaying a guard ring within an integrated circuit design having logic devices, said method comprising:

determining positions of said logic devices within said integrated circuit design;

incorporating said guard ring into said integrated circuit design; and

displaying said logic devices and said guard ring graphically, semantically, or symbolically in a single display,

wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol comprising displaying parameters, including at least one of a type of circuit, a type of said guard ring, and an efficiency of said guard ring.

2. (Canceled).

3. (Previously Presented) The method in claim 1, wherein said displaying of said parameterized symbol displays parameters including the type of circuit and the type of guard ring.

4. (Previously Presented) The method in claim 1, wherein said displaying of said parameterized symbol displays parameters including the efficiency of said guard ring.

5. (Original) The method in claim 1, wherein said displaying of said logic devices and said guard ring graphically comprises illustrating relative positions of said logic devices and said guard ring.

6-12. (Canceled).

13. (Currently Amended) A method of displaying at least one guard ring within a hierarchical integrated circuit design having logic devices, said method comprising:

establishing positions of said logic devices within a portion of said hierarchical integrated circuit design;

incorporating said guard ring into said portion of said hierarchical integrated circuit design; and

displaying said portion of said integrated circuit design as a cell having a guard ring within said hierarchical integrated circuit design, wherein said displaying of said portion of said integrated circuit design comprises symbolically displaying a parameterized symbol comprising displaying parameters, including at least one of a type of circuit, a type of said guard ring, and an efficiency of said guard ring.

14. (Canceled).

15. (Previously Presented) The method in claim 13, wherein said displaying of said parameterized symbol displays parameters including the type of circuit and the type of guard ring.

16. (Previously Presented) The method in claim 13, wherein said displaying of said parameterized symbol displays parameters including the efficiency of said guard ring.

17. (Original) The method in claim 13, wherein said displaying of said portion of said integrated circuit design comprises graphically illustrating relative positions of said logic devices and said guard ring.

18-24. (Canceled).

25. (Currently Amended) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of

displaying a guard ring within an integrated circuit design having logic devices, said method comprising:

determining positions of said logic devices within said integrated circuit design;

incorporating said guard ring into said integrated circuit design; and

displaying said logic devices and said guard ring graphically, semantically, or symbolically in a single display, wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol comprising displaying parameters, including at least one of a type of circuit, a type of said guard ring, and an efficiency of said guard ring.

26. (Canceled).

27. (Previously Presented) The program storage device in claim 25, wherein said displaying of said parameterized symbol displays parameters including the type of circuit and the type of guard ring.

28. (Previously Presented) The program storage device in claim 25, wherein said displaying of said parameterized symbol displays parameters including the efficiency of said guard ring.

29. (Original) The program storage device in claim 25, wherein said displaying of said logic devices and said guard ring graphically comprises illustrating relative positions of said logic devices and said guard ring.